

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Masahiro ISHIDA et al.                          Art Unit :  
Serial No.:    Examiner :  
Filed : Herewith  
Title : METHOD AND APPARATUS FOR DEFECT ANALYSIS OF SEMI-  
CONDUCTOR INTEGRATED CIRCUIT

Assistant Commissioner for Patents  
P. O. Box 1450  
Alexandria, VA 22313-1450

**PRELIMINARY AMENDMENT**

Prior to consideration on the merits, please amend the application as follows and consider the included remarks.

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PATENT TRADEMARK OFFICE